II. LISTING OF THE CLAIMS

The following listing of the claims is a courtesy copy only, as no claims have been amended by this response:

1. (Original) A semiconductor device structure comprising:

at least two active regions having different surface directions, each active region including one of a plurality of nFETs and a plurality of pFETs, and

wherein a gate electrode orientation is such that the nFETs and the pFETs are substantially parallel to each other.

2. (Original) The structure of claim 1, wherein the pFETs are located in an active region with a current flow in a <110> surface direction, and the nFETs are located in an active region with a current flow in a <100> surface direction.

3. (Original) The structure of claim 1, wherein the pFETs are located in an active region with a (110) surface orientation and a <111> surface direction, and the nFETs are located in an active region with a (100) surface orientation and a <110> surface direction.

4. (Original) The structure of claim 1, further comprising means for applying:

a compressive stress in a longitudinal direction with respect to a current flow of the pFET and a transverse direction with respect to a current flow of the nFET; and

a tensile stress in a longitudinal direction with respect to a current flow of the nFET and a

transverse direction with respect to a current flow of the pFET.

5. (Original) A method of forming a semiconductor device structure, the method comprising the steps of:

bonding a first wafer having a first surface direction atop a second wafer having a different second surface direction;

forming an opening through the first wafer to the second wafer; and

forming a region in the opening coplanar with a surface of the first wafer, wherein the region has the second surface direction.

6. (Original) The method of claim 5, further comprising the steps of:

implanting an oxygen; and

annealing to form a buried oxide layer.

7. (Original) The method of claim 6, further comprising the step of forming a first type gate electrode on the region, and a second type gate electrode on another region of the first wafer, and all of the gate electrodes are substantially parallel to one another.

8. (Original) The method of claim 7, wherein the first gate electrode includes a pFET, and the second gate electrode includes an nFET.

9. (Original) The method of claim 8, further comprising the step of applying at least one of a filled trench configuration and at least one film to provide:

a compressive stress in a longitudinal direction with respect to a current flow of the pFET and a transverse direction with respect to a current flow of the nFET; and

a tensile stress applied in a longitudinal direction with respect to a current flow of the nFET and a transverse direction with respect to a current flow of the pFET.

10. (Original) The method of claim 5, wherein each wafer includes a silicon layer on an insulator layer, and the opening forming step includes forming the opening to the silicon layer of the second wafer.

11. (Original) The method of claim 10, wherein the region forming step includes epitaxially growing silicon in the opening, and planarizing the silicon.

12. (Original) The method of claim 5, wherein the opening forming step includes forming a sidewall spacer along the opening.

13. (Original) The method of claim 5, wherein the first surface direction is a <100> surface direction and the second surface direction is a <110> surface direction.

14. (Original) The method of claim 5, wherein the first surface direction is a <110> surface direction and the second surface direction is a <111> surface direction.

15. (Original) The method of claim 5, wherein the first wafer has a first surface orientation and the second wafer has a different second orientation, and the region has the second surface orientation.

16. (Original) The method of claim 5, wherein the first surface direction and the second surface direction are selected to degrade mobility.

17. (Original) A method of forming a semiconductor device structure, the method comprising the steps of:

bonding a first wafer having a first surface direction and a first surface orientation atop a second wafer having a different second surface direction and a different second surface orientation;

forming an opening through the first wafer to a silicon layer of the second wafer;

generating a silicon in the opening to a surface of the first wafer, wherein the silicon has the different second surface orientation;

forming a plurality of pFETs on the silicon, and a plurality of nFETs on another region of the first wafer, wherein gate electrodes of the FETs are substantially parallel to one another; and

applying at least one of a filled trench configuration and at least one process to provide:

a compressive stress in a longitudinal direction with respect to a current flow of the pFETs and a transverse direction with respect to a current flow of the nFETs; and

a tensile stress in a longitudinal direction with respect to a current flow of the nFETs and a transverse direction with respect to a current flow of the pFETs.

18. (Original) The method of claim 17, further comprising the steps of implanting oxygen; and annealing to form a buried oxide layer prior to the FET forming step.

19. (Original) The method of claim 17, wherein each wafer includes a silicon layer on an insulator layer, and the opening forming step includes forming the opening to the silicon layer of the second wafer.

20. (Original) The method of claim 17, wherein the region generating step includes epitaxially growing silicon in the opening, and planarizing the silicon, and the opening forming step further includes forming a sidewall spacer along the opening.